FPGA Implementation of a Spiking Neural Network for Pattern Matching

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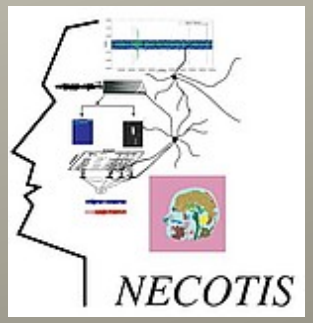


Pattern matching

- What is pattern matching ?
  - Identification and association of patterns in a set of input data
- How is it implemented ?
  - The Oscillatory Dynamic Link Matcher (ODLM)
    - Image segmentation and comparison [1]
    - Monophonic sound source separation [2]
- Why port it to hardware ?
  - Versatility of the ODLM on an embedded system

[1] Pichevar et al., Neurocomputing (2006)
[2] Pichevar and Rouat, Neurocomputing (2007)

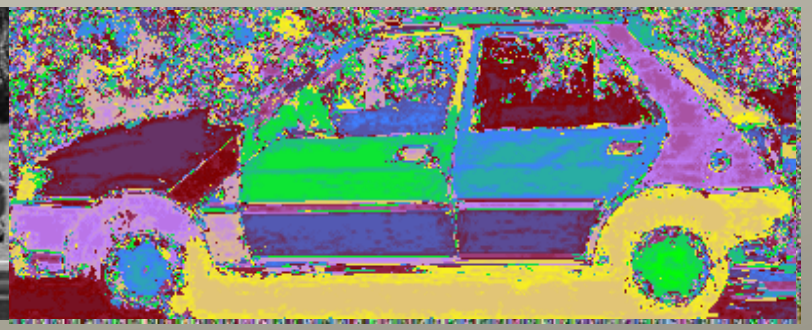
The ODLM

- Signal processing task determines
  - the size of the network
  - the topology of the network

- Image segmentation

Original image

State of the network

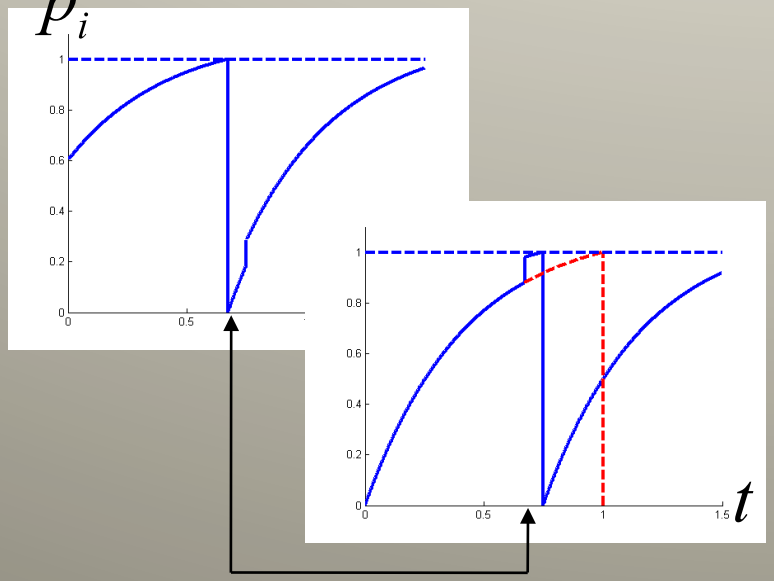


ODLM: Oscillatory Dynamic Link Matcher

The ODLM

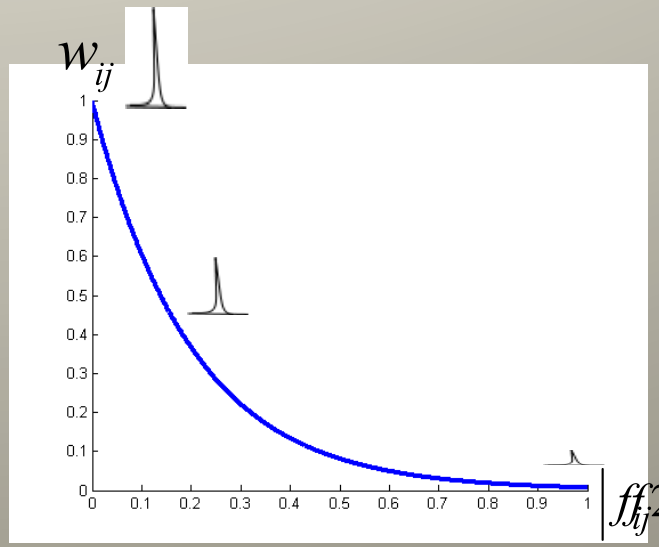
- Leaky integrate and fire neuron model
  - Membrane model

$$p_i = \frac{I_0}{\Pi}(1) \quad 2t/\Pi$$



  - Synaptic weights

$$w_{ij} =$$



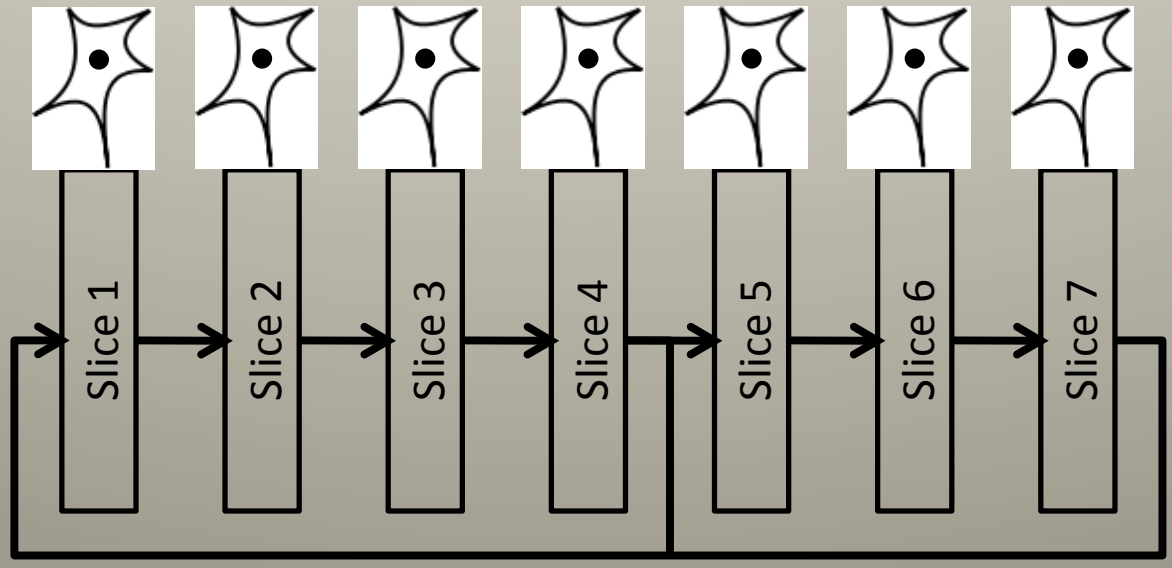
ODLM: Oscillatory Dynamic Link Matcher

Main focus points

- Scalability
  - Adapt the size of the network to the application at hand
- Flexibility
  - Allow the implementation of networks of any topology
- Parallelism
  - Perform batch propagation of simultaneous spikes

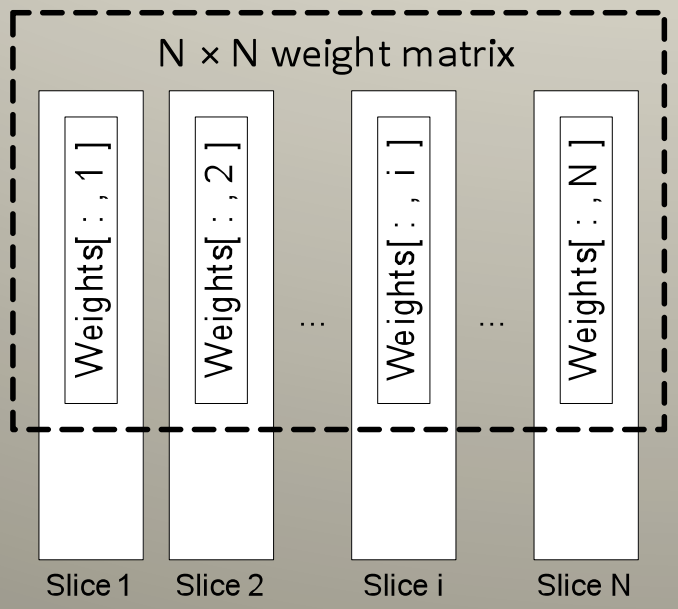
Scalability

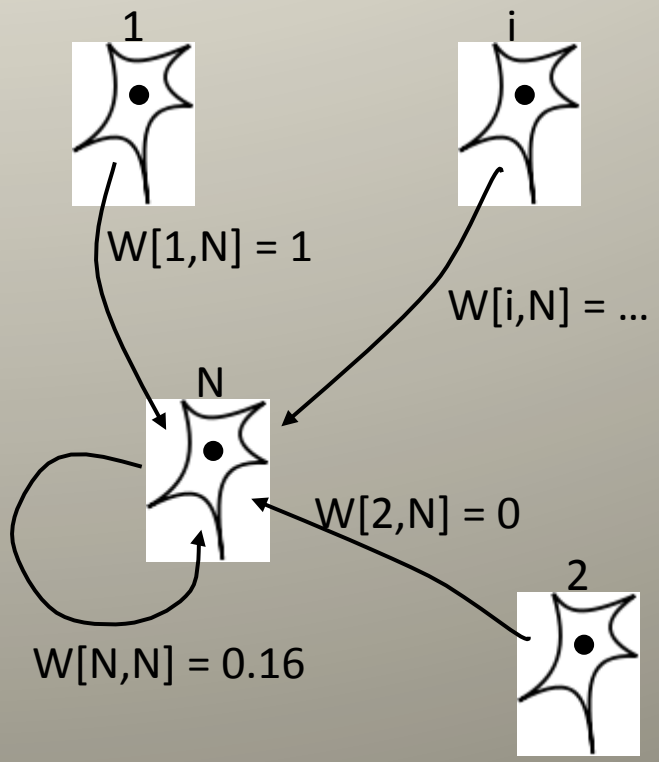
- Bit-slice architecture
  - Layout friendly, easy placement and routing
  - Each slice implements one neuron



Flexibility

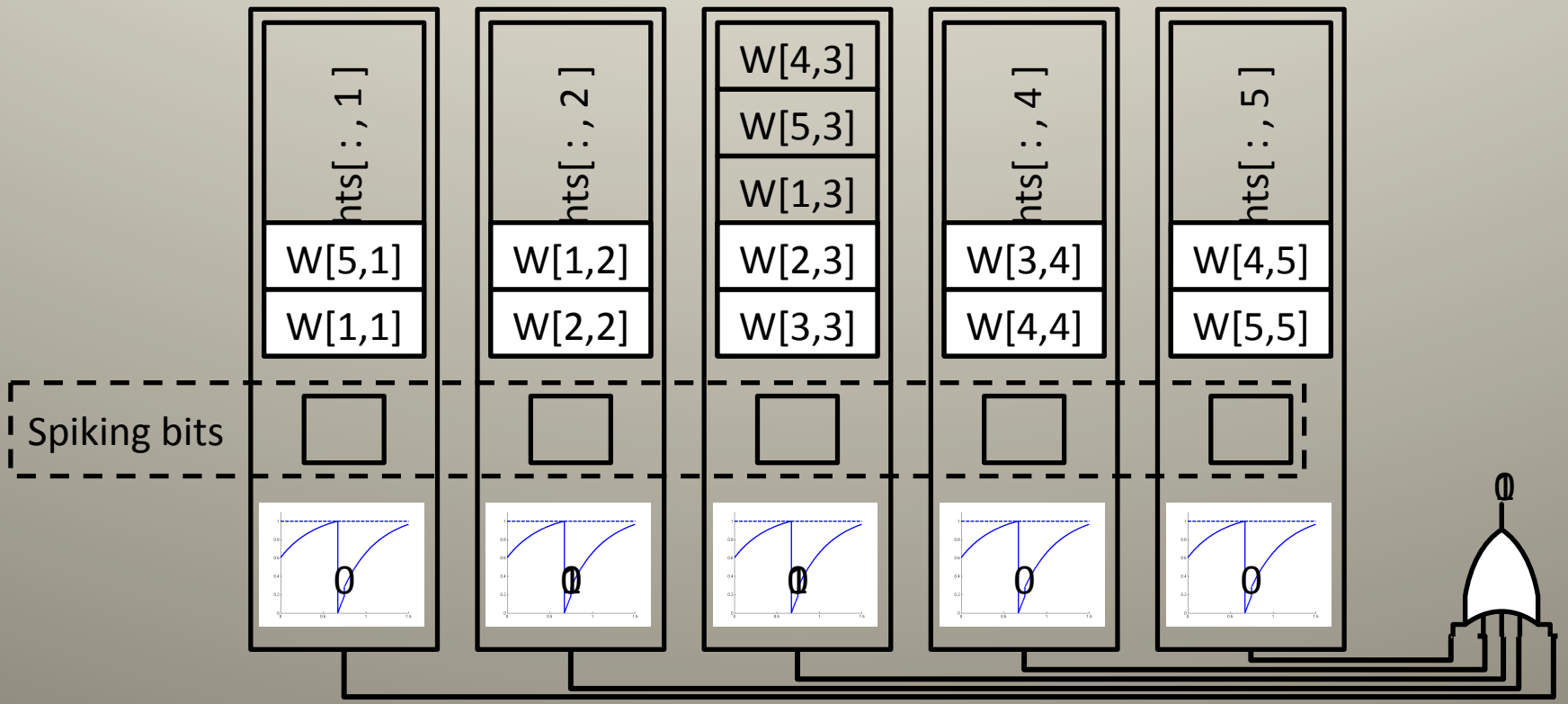
- Store the weights as if fully connected
  - Slice *i* stores the weights from all the neurons to neuron *i*





Parallelism

- Update of the membrane potentials
- Propagation of simultaneous spikes



Performance

- Xilinx XC5VSX50T Virtex-5 FPGA clocked at 100 MHz
  - 648 neurons and 419904 synapses
- Processing speed
  - Full synchronization: 6M spikes/s
  - No synchronization: 9.6k spikes/s
- Image segmentation
  - 27×24 pixel image
  - 8-neighbor topology
  - 648 neurons
  - 2 seconds of processing
- Image comparison
  - 90×30 pixel images
  - Fully connected topology
  - 112 neurons
  - 550 ms of processing

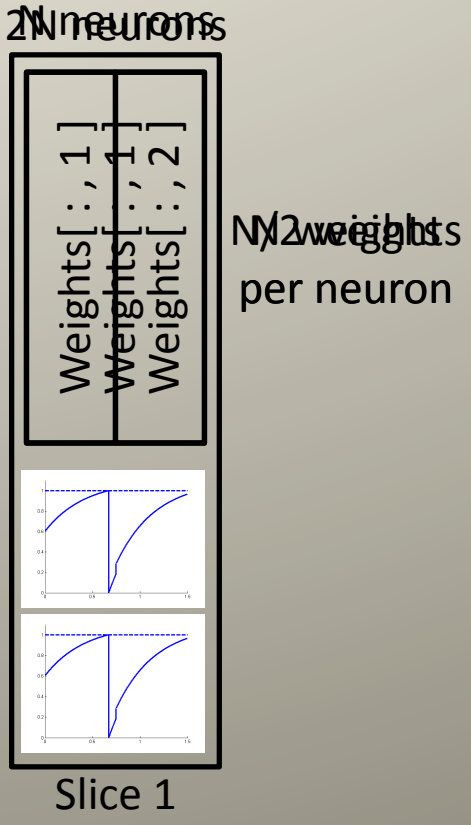
Performance

- Compared to other hardware spiking neural networks [3]
  - Better flexibility
  - Lower performance
- Compared to software ODLM
  - Low number of neurons
  - Initialization method

[3] Vega-Pineda et al., IEEE IJCNN Proceedings, 2006.

Future work

- Improve support for various regular topologies
  - Slices should
    - handle several neurons
    - store fewer weights per neuron
  - A network of 52488 neurons with 8-neighbor connectivity (81 neurons / slice)



Conclusion

- Bit-slice architecture
  - + Scalable
  - + Placement and routing on ASIC
- Square weight matrix
  - + Flexible
  - + Plasticity/learning
  - − Burdensome

ASIC: Application-specific integrated circuit

Conclusion

- Level of synchrony affects processing speed
  - + Exploits the synchrony in the network
  - − Random initialization of potentials
- Performance
  - + Better flexibility
  - − Lower processing speed
- Spike detection signal
  - − Critical path

Summary

- FPGA implementation of a spiking neural network for pattern matching
  - Processes simultaneous spikes in parallel
  - Can be ajusted in size
  - Can perform different signal processing tasks
  - Can be improved to yield better performance with networks of regular topology